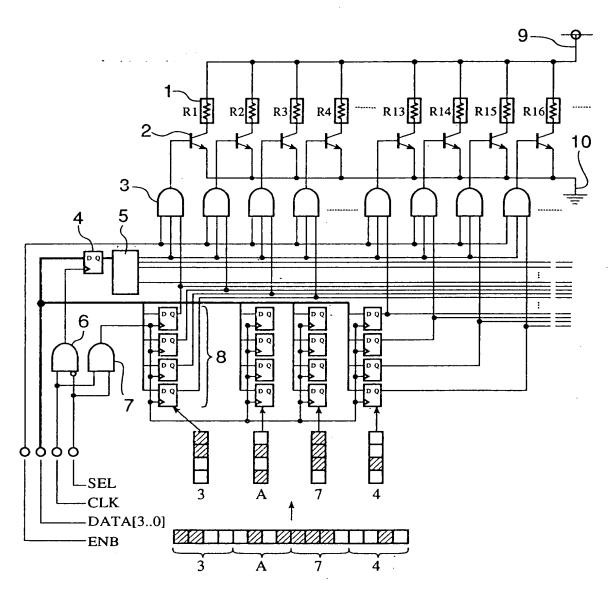
FIG. 1



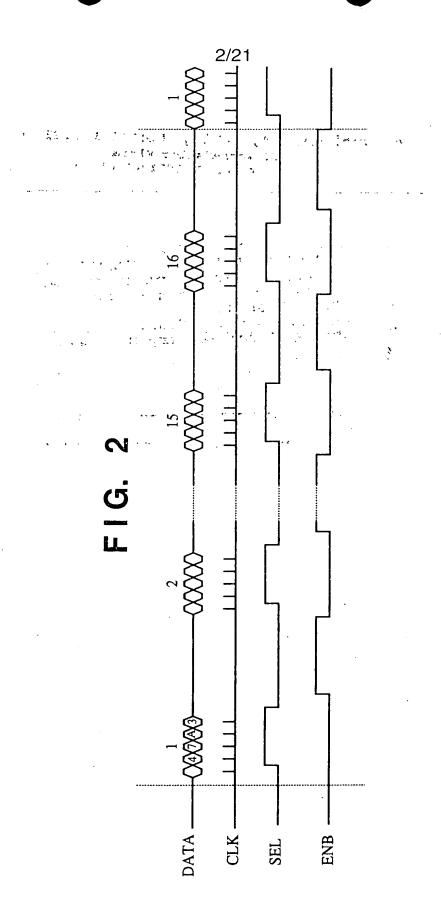
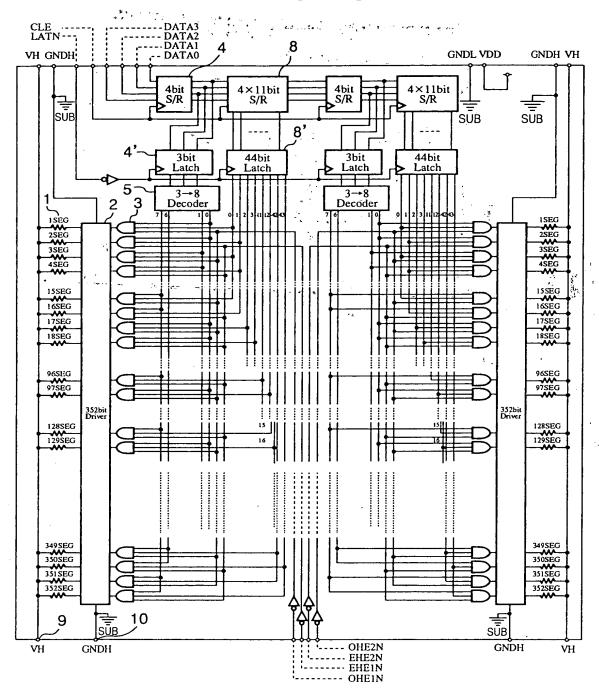
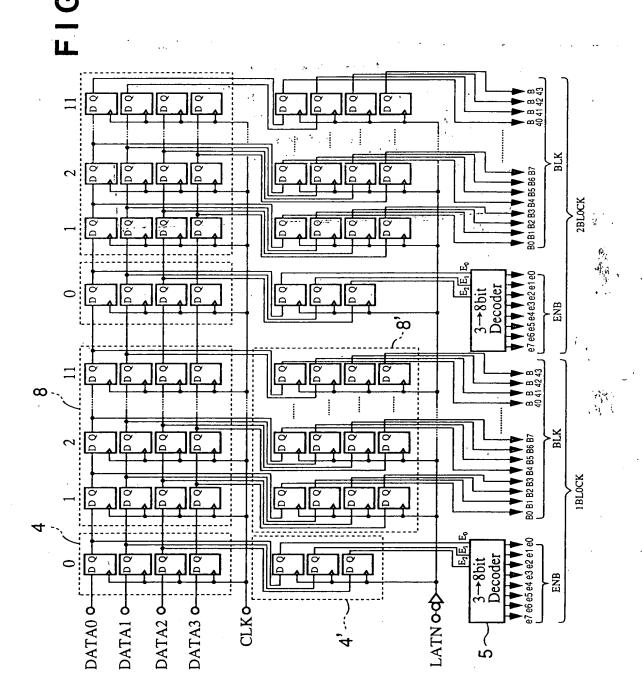
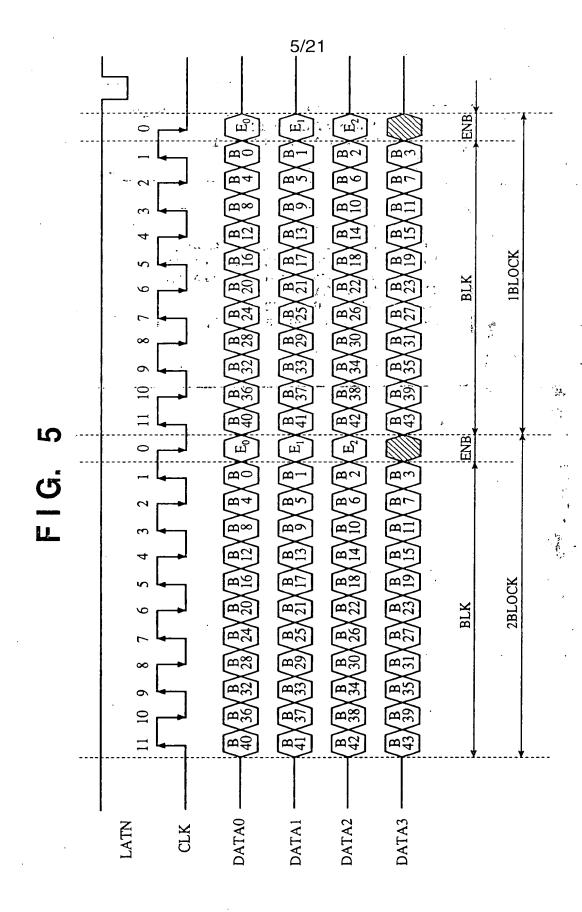


FIG. 3

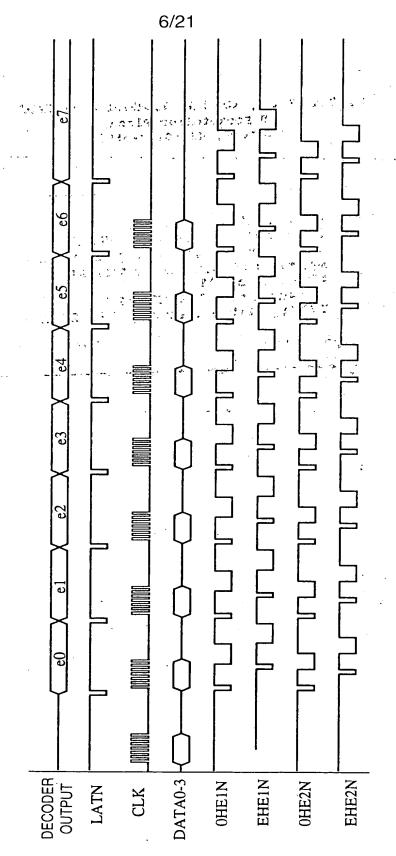




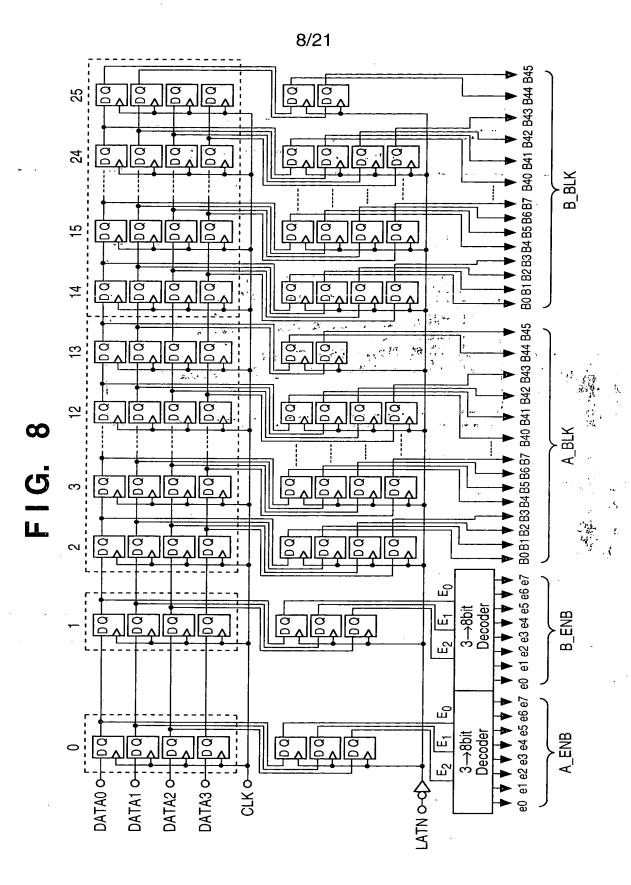
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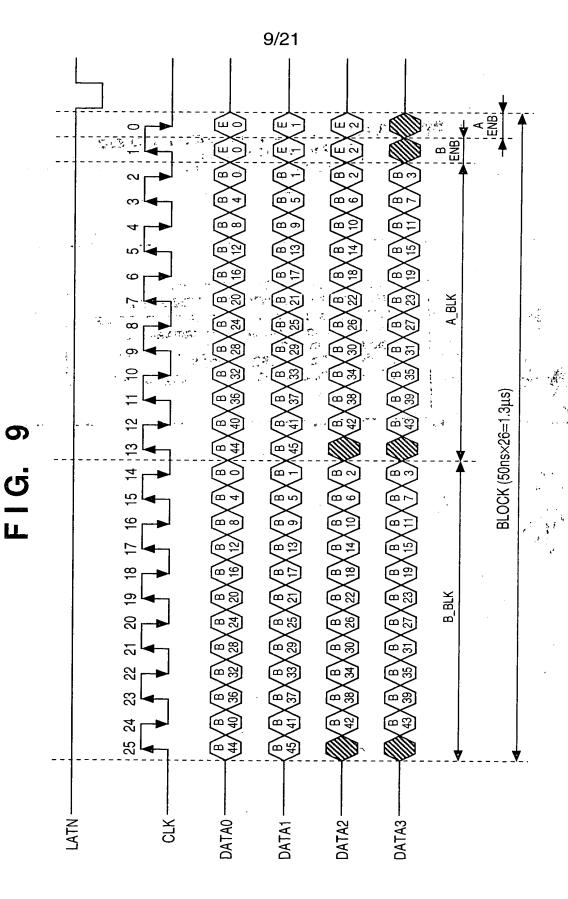


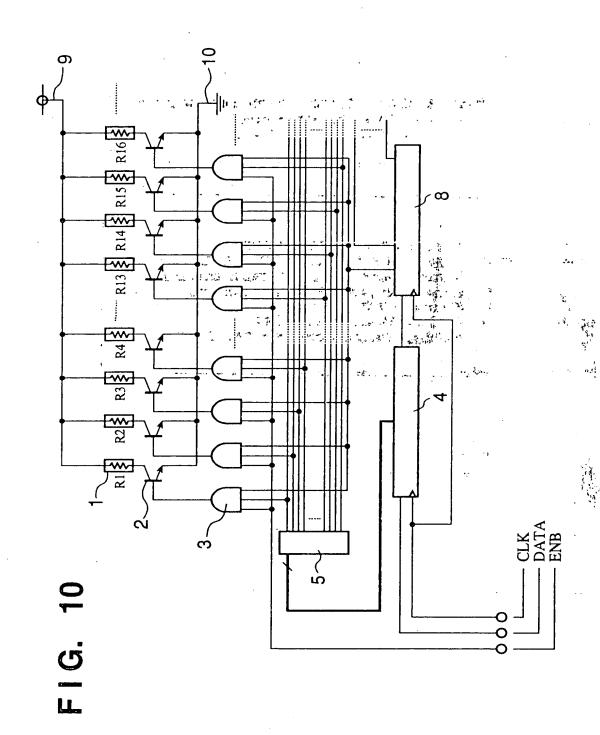
F G. 6

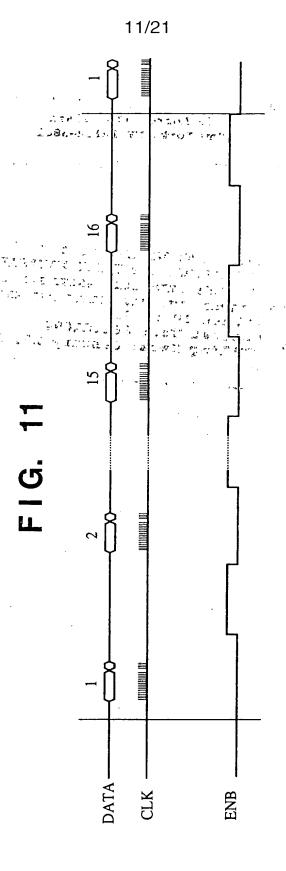


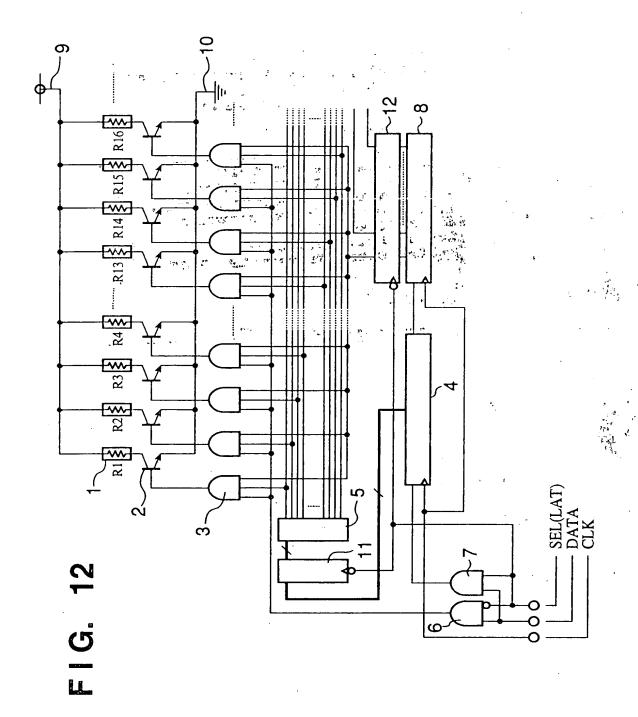
7/21 FIG. ---- DATA3 ---- DATA2 ---- DATA1 CLE LATN 8 (ODATA) GNDL VDD GNDH VH VH GNDH 4×12bit∐s 4bit 4bit 4×12bit S/R S/R S/R -S/R -SŪB J SÜB 8' \(\frac{1}{SUB} \) 4' 8' 3bit Latch 3bit Latch 46bit Latch 46bit Latch 3→8 3→8 Decoder Decoder 2 A1SEG A2SEG A3SEG B1SEG B2SEG B3SEG A4SEG B4SEG A15SEG A16SEG A17SEG A18SEG B15SEG B16SEG B17SEG B18SEG B80SEG B81SEG A80SEG A81SEG 368bit Driver 368bit Driver A160SEG A161SEG B160SEG B161SEG B240SEG B241SEG A240SEG A241SEG B365SEG B366SEG B367SEG B368SEG A367SEG ≟ SŪB SÜB OHE2N EHE2N EHE1N OHE1N **GNDH** GNDH VH ġ 10

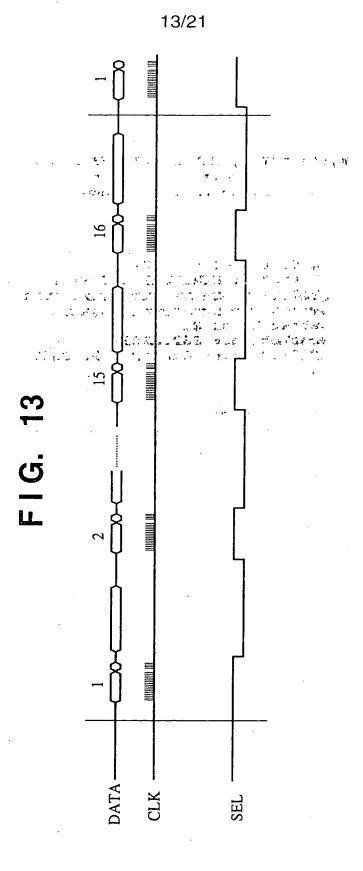


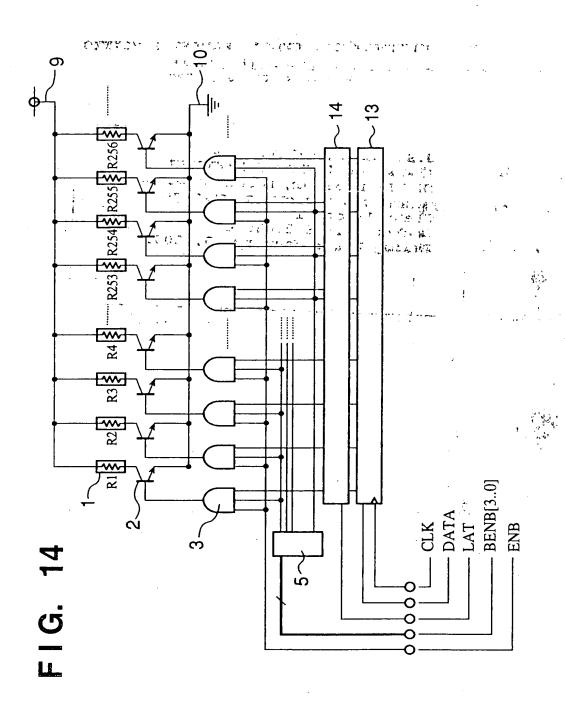


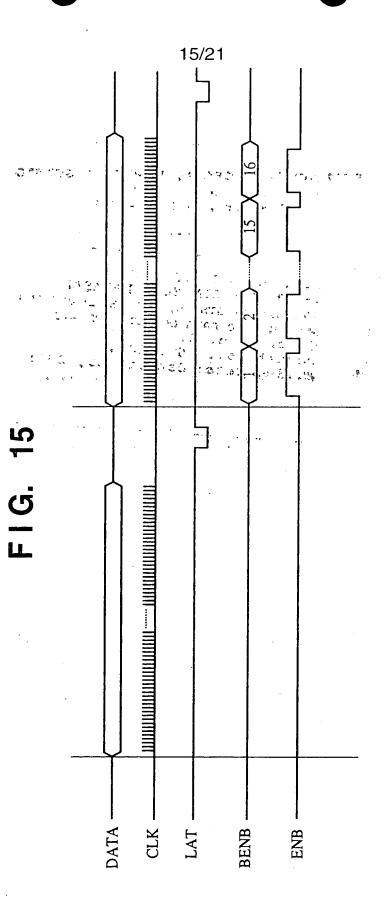


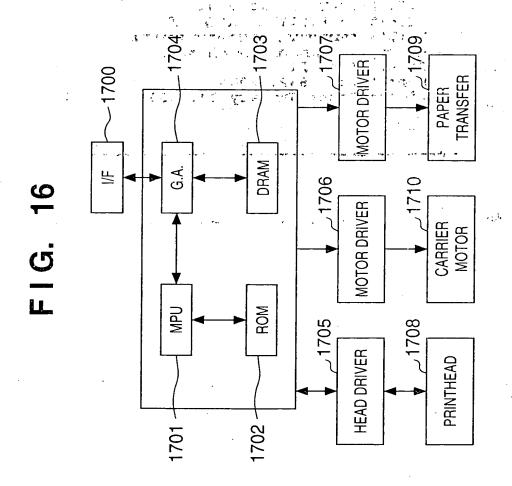




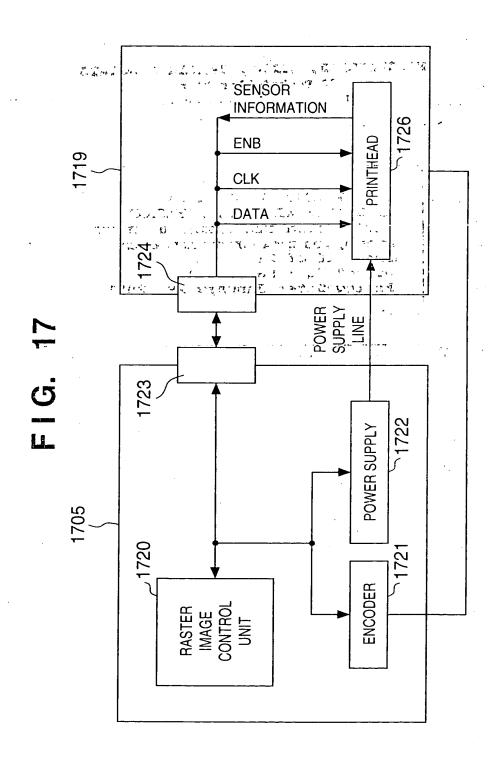


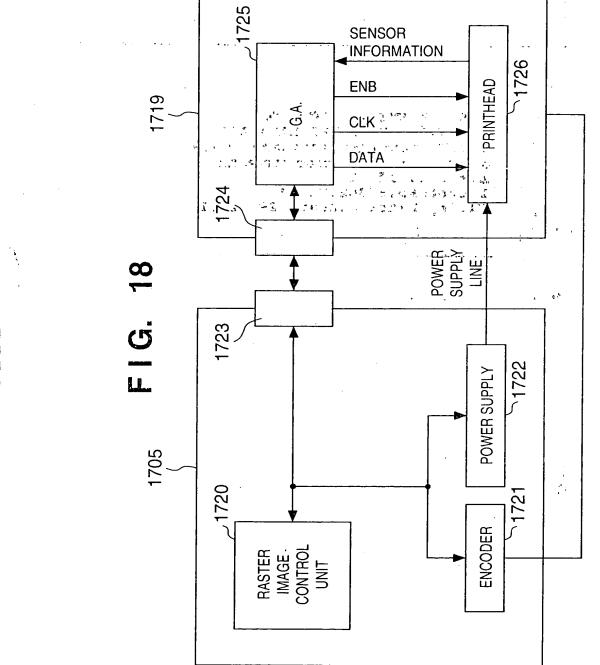












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